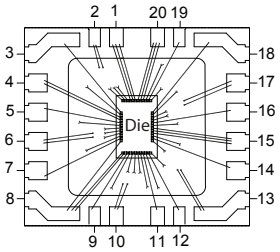
How Does PotatoSemi Kill inside Noise Of IC ?

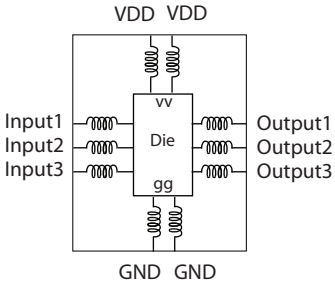
Voltage mode differential Logic. New Patent IP.

Improved CMOS logic by using high frequency noise cancellation technology

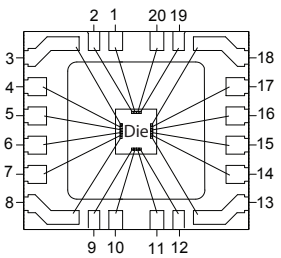
Potato IC



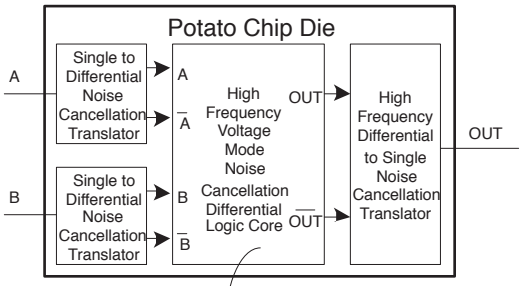
High Frequency Noise Cancellation bonding diagram

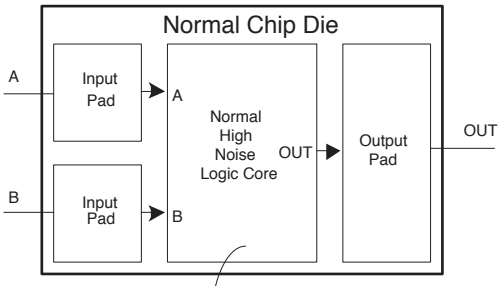


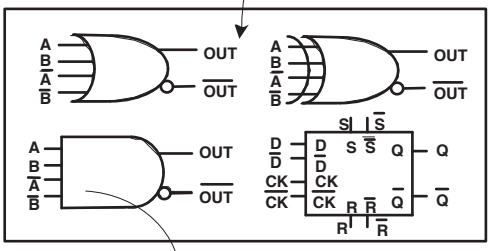
Normal IC

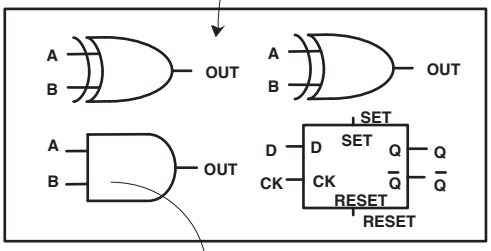


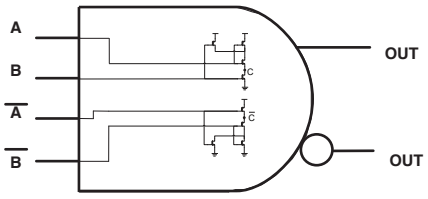
Normal IC bonding diagram

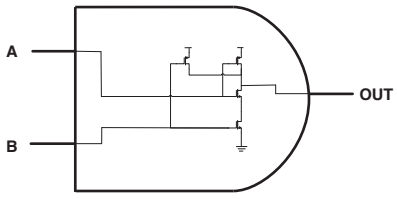


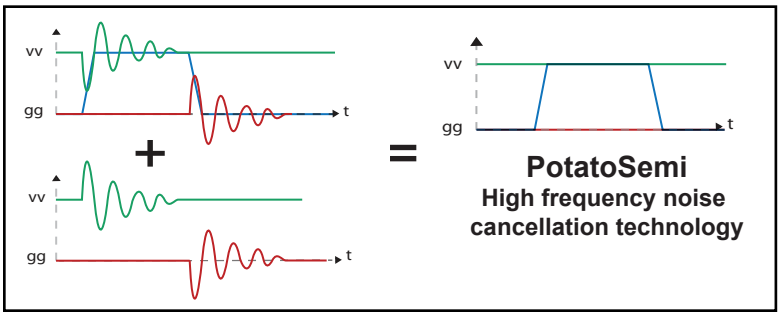


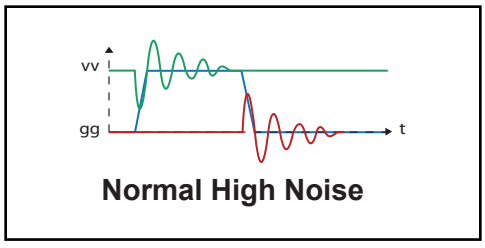












Contact Potato Semiconductor for IP or detail.

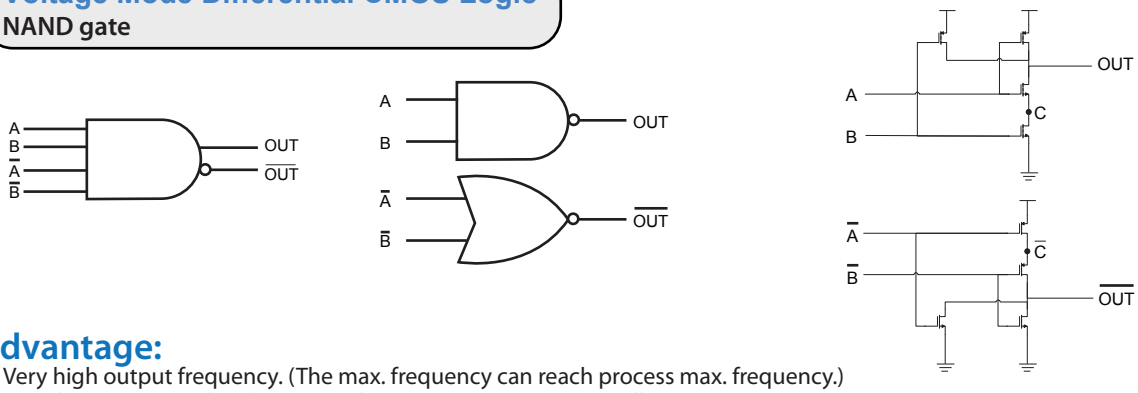
Noise Cancellation Logic

Voltage Mode Differential Logic

Improved CMOS logic by using high frequency noise cancellation technology

Voltage Mode Differential CMOS Logic

NAND gate



Advantage:

1. Very high output frequency. (The max. frequency can reach process max. frequency.)
2. Switching noise can be eliminating by note to note noise cancellation.
   (Noise from note A & noise from note A bar will cancel each other. Noise from note B & noise from note B bar will cancel each other. Noise from note C & noise from note C bar will cancel each other. Noise from note out & noise from note out bar will cancel each other.)
3. Rail to rail output signals.
4. Without switching noise, logic output signal can be much stronger then other logic output signal.
5. Low jitter.
6. Output signals can drive long distance.
7. No error bit.
8. No static current.
9. Design is very similar to normal CMOS logic. It can be used for high frequency & high performance VLSI design.

Disadvantage:

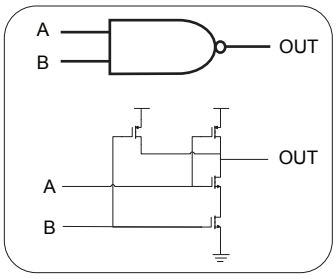
More complicate design then normal CMOS logic
Bigger die size then normal low speed CMOS logic.

Example:

Potato Semiconductor ICs are using this technology such as
GHz 74 series logic, clock buffer, bus switch, signal translator.

Normal static CMOS Logic

NAND gate



Advantage:

1. Simple.
2. Small Die size.
3. No static current

Disadvantage:

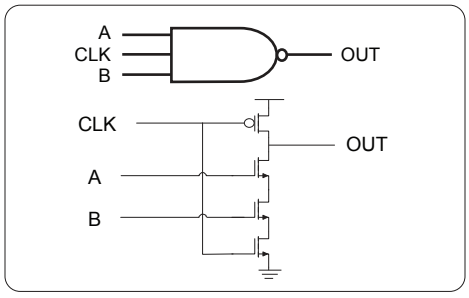
1. High switching noise.
2. Low operating frequency.
3. Higher error bit rate.
4. Higher jitter.
5. higher propagation delay.
6. weak output signal.

Example:

Most low frequency logic ICs are using this technology such as regular 74 series CMOS logic.

Dynamic Logic

Dynamic NAND gate



Advantage:

1. Higher output frequency then normal logic
2. Less input capacitance & less switching noise from input A & B then normal static logic.

Disadvantage:

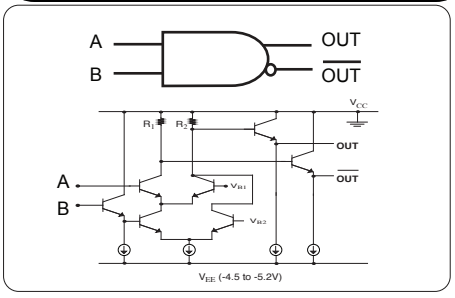
1. High Power consumption.
2. Can not run lower clock frequency
3. Output signal is switching all the time.

Example:

Most high clock frequency ASIC ICs are using this technology such as graphic chips.
They usually work with a big fan.

Current mode differential Logic

Current Mode Differential NAND gate



Advantage:

1. High output frequency.
2. Low noise.
3. Low jitter.

Disadvantage:

1. Current source design with high static current.
2. Complicate design.
3. Difficult to design a perfect current source.
4. Need many extra components such as 50 ohm loading resistors.

Example:

Most high frequency outputs are using this technology such as ECL logic, PECL, LVDS, CML etc.

Bring Power into ICs

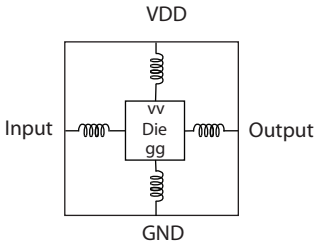
How does decupling capacitor work?

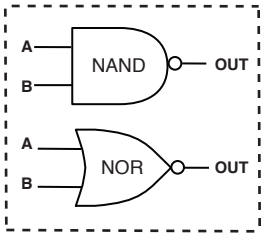
All electronics engineers know decupling capacitor.
However, do you know how to make them working properly?
There are four examples show below.
Only last circuit can clean noise.
Only opposite noise plus decupling capacitor working together can release electronics from capacitor & clean up IC & system noise.

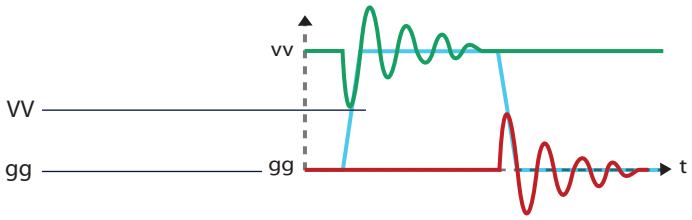
Example 1

Normal CMOS logic without decupling capacitor

Power voltage between vv & gg will change because of the switching noise.



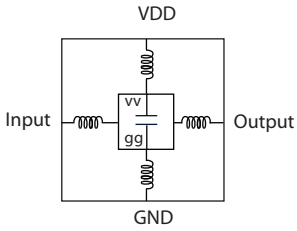


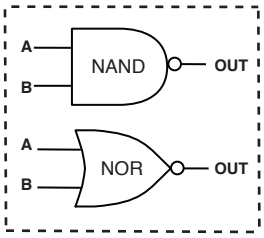


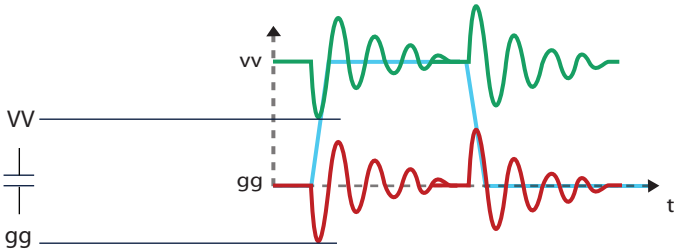
Example 2

Normal CMOS logic with decupling capacitor

Decupling capacitor will maintain power voltage between vv & gg, but it can not clean noise.



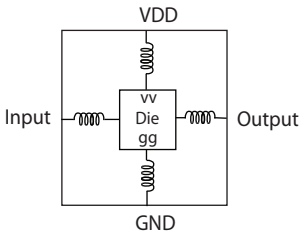


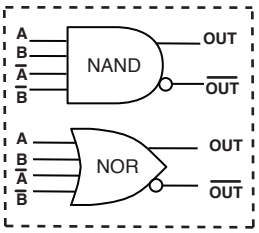


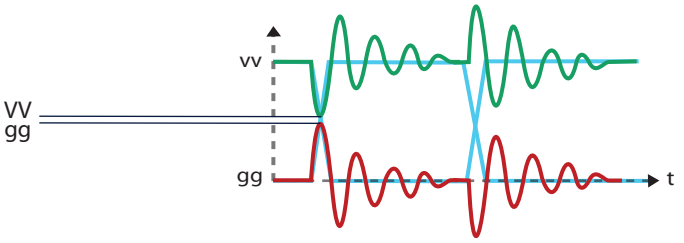
Example 3

Voltage mode differential logic without decupling capacitor

Power voltage between vv & gg will change because of the positive noise & its opposite noise.



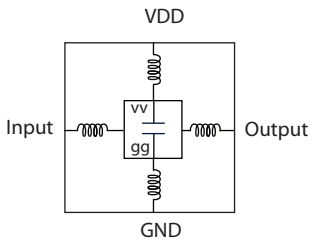


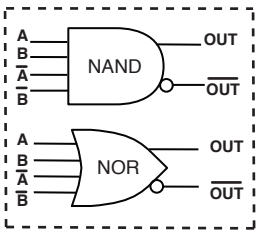


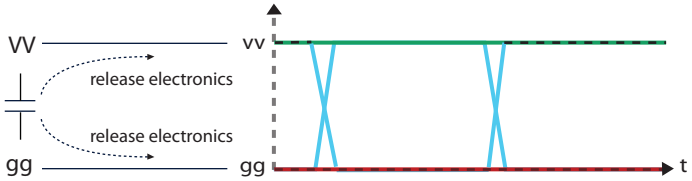
Example 4 (Potato technology)

Voltage mode differential logic with decupling capacitor

Positive noise & its opposite noise will cancel each other.



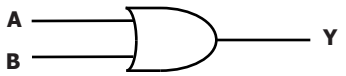




How does the New Technology work ?

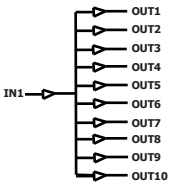
By using our special IO interface, logic cells & design rule, we can convert most of existing Logic chips into much higher frequency than it was before. After we convert the standard chips, all chips become much more reliable, much less noise and much higher running frequency.

Compare to 74 Series Logic



	PotatoSemi	TI	Fairchild	Renesa	NXP
Device	PO74G32A	SN74ALVC32	74LVX32	HD74LV32A	74ALVC32
Vcc	1.65V ~ 3.6V	1.65V ~ 3.6V	2V - 3.6V	2V ~ 5.5V	1.65V ~ 3.6V
Max. Frequency	2 GHz	200 MHz	200 MHz	200 MHz	200 MHz
Propagation delay (Max)	1.5 ns	2.8 ns	7.5 ns	6.5 ns	2.8 ns
Low input capacitance	4.0 pf	4.0 pf	4.0 pf	4.0 pf	3.5 pf

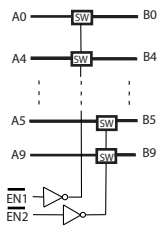
Compare to Clock Buffers



	PotatoSemi	Pericom	IDT	ICS	Cypress	NXP
Device	PO49FCT3807B	49FCT3807	74FCT3807E-D	MK3807-01	CY2CC810	PCK3807A
Vcc	1.65V ~ 3.6V	3.3V	3.3V	3.3V	2.5V or 3.3V	2.5V or 3.3V
Max. Frequency	800M Hz	156 MHz	166 MHz	100MHz	250MHz	150 MHz
pin to pin skew	80 ps	250 ps	100 ps	350 ps	380 ps	120 ps
Pulse skew	250 ps	250 ps	250 ps	350 ps	200 ps	300 ps
Propagation delay (Max)	2.0 ns	2.5 ns	2.0 ns	3.8 ns	3.5 ns	2.5 ns
Low input capacitance	3 pf	3.0 pf	3 pf	5 pf	3 pf	3 pf

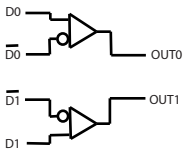
How does the New Technology work ?

Compare to GHz Bus Switch



	PotatoSemi	Pericom	TI	Fairchild
Device	PO3B1000A	PI3CH1000	SN74CB3Q3384A	FST3384
Vcc	1.65V ~ 3.6V	2.5V / 3.3V	2.3V ~ 3.6V	4.0V~5.5V
Wide Bandwidth (-3db) AC	1.2GHz	500 MHz	500 MHz	N/A
Near-Zero Delay	Yes	Yes	Yes	Yes
Special design for differential signals	Yes	No	No	No
Ron (Max.) DC	18Ω	8 Ω	9 Ω	20Ω
Con (typ.)	7.9 pf	6.4 pf	10 pf	5 pf
Ultra-Low Quiescent Power (Typ.)	0.1μA	N/A	1000 μA	0.1μA
Quiescent Power (Max.)	3 μA	800 μA	2000 μA	3 μA

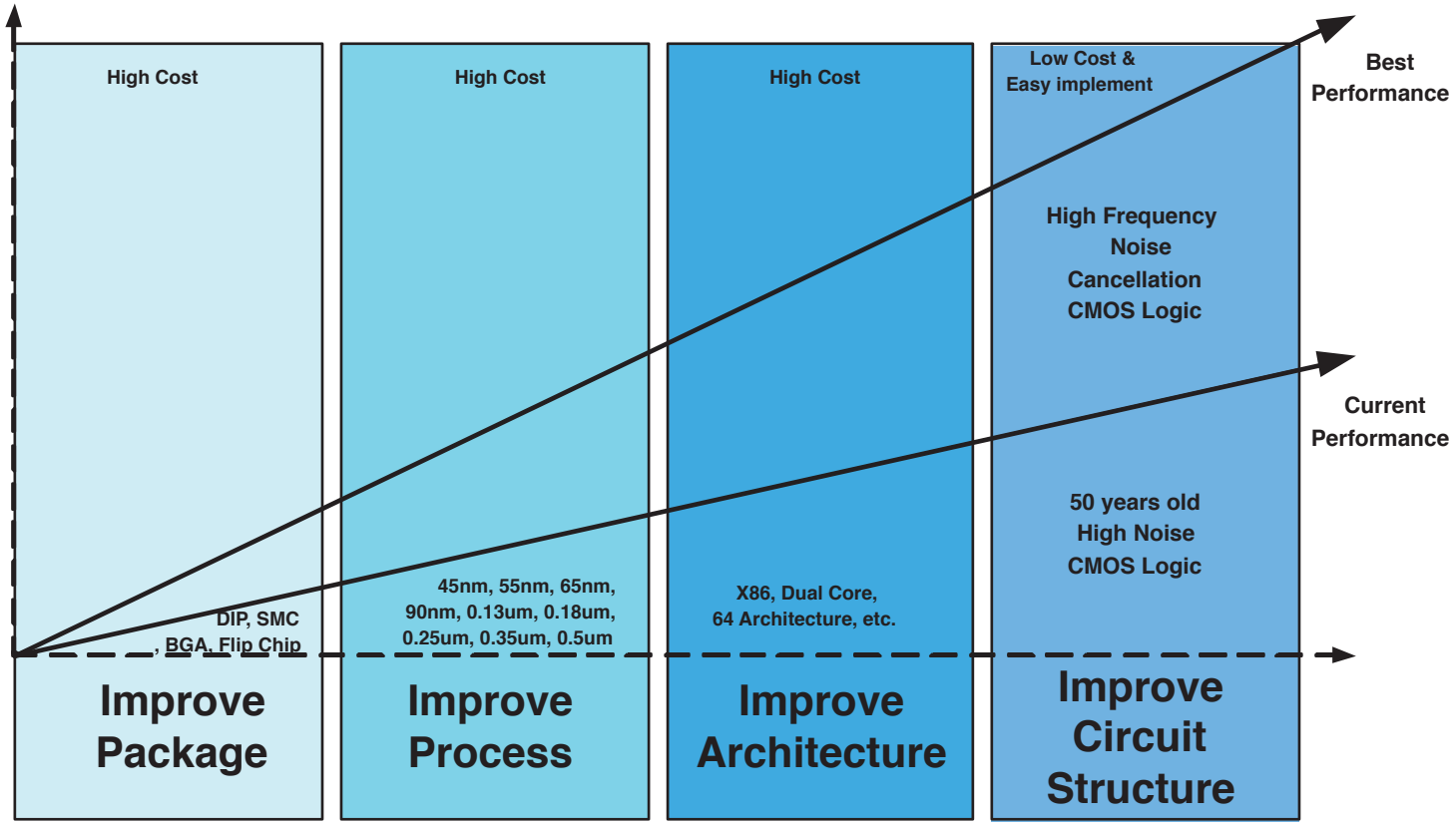
Compare to GHz Translator



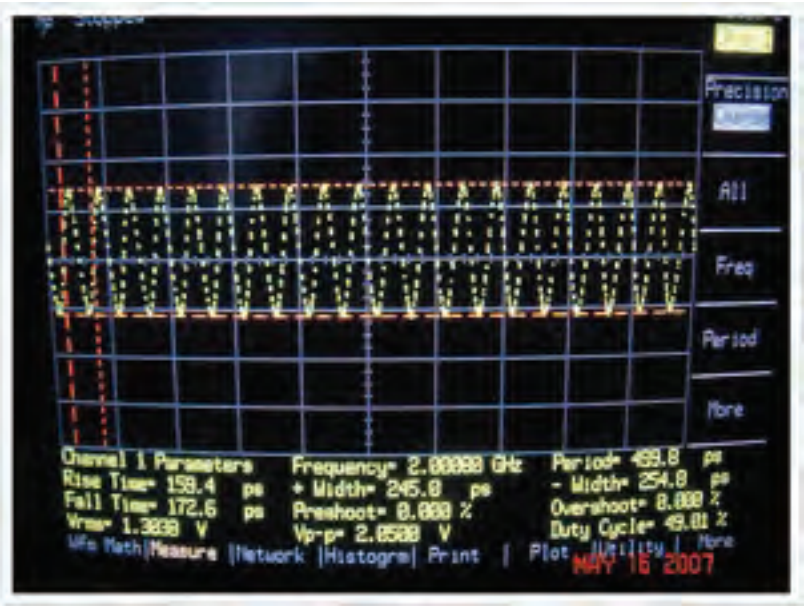
	PotatoSemi	OnSemi	Micrel	TI	ICS
Device	PO100HSTL23A	MC100EPT23-D	SY89323L	SN65LVDS9637D	ICS83023I
Vcc	2.4V ~ 3.6V	3V-3.6V	3V-3.6V	3V-3.6V	3V-3.6V
Max. Frequency	1 GHz	275 MHz	275 MHz	200 MHz	350 MHz
pin to pin skew	150 ps	125 ps	300 ps	400 ps	60 ps
output skew (different package)	300 ps	500 ps	500 ps	1000 ps	500 ps
propagation delay (Max)	1.8 ns	2.4 ns	2.5 ns	3 ns	2.4 ns

Next Generation Logic Cells

The best way to improve an IC is from the core circuit structure!



GHz CMOS Output



POTATO

potato Semiconductor Corporation

CMOS technology has been widely used for more then 50 years. It delivers the low cost with high yield. However, because of the unbalanced CMOS structure, it will generate high noise into Power & ground. From the past 50 years of IC history, our GHz CMOS output driver is the only technology that you can kill your chip internal ground and power noise without scarifies your output performance. Because of this noise cancellation technology, our output frequency can be 7 to 10 times faster then anyone else in this world. In addition, because of this low noise tech nology, any ICs with our output drivers can deliver the accuracy without any error.

The example shows the output signal from our standard logic PO74G32A. The VCC is 3V. The output frequency from the measurement is 2GHz with probe loading. The max frequency will be more than 2GHz. Vp-p is 2.075V. Vhigh is 2.175V. Vlow is 100mV.